IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kazuhiro Nakajima

Serial No.: 10/649,833 Group Art Unit: 2817

Filed: August 28, 2003 Examiner: Shingleton, Michael B.

For: TEST METHOD AND APPARATUS FOR VERIFYING FABRICATION OF TRANSISTORS IN AN INTEGRATED CIRCUIT

Honorable Commissioner of Patents
Alexandria, VA 22313-1450

SUBMISSION OF REPLACEMENT DRAWING
SHEETS INCLUDING DRAWING CORRECTIONS

Sir:

Submitted herewith is a replacement drawing sheet including a proposed drawing correction. Figure 1 is proposed to be corrected by correcting the symbols representing the three n-type MOSFETs 24.

A marked drawing having the correction in red is also attached..

Approval and acknowledgment of receipt are respectfully requested.

Respectfully Submitted,

Date: May 23, 2005

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